In the Claims:

1. (Currently Amended) ~~Method~~A method for fabricating a spacer structure, the method comprising ~~the steps of~~:

a) forming a gate insulation layer ~~(2)~~ having a gate deposition-inhibiting layer ~~(2A)~~, a gate layer ~~(3)~~ and a covering deposition-inhibiting layer ~~(4)~~ on a semiconductor substrate ~~(1)~~;

b) patterning the gate layer ~~(3)~~ and the covering deposition-inhibiting layer ~~(4)~~ in order to form gate stacks ~~(G)~~; and

c) depositing an insulation layer ~~(6)~~ selectively with respect to the deposition-inhibiting layers ~~(2A, 4)~~ to form the spacer structure.

2. (Currently Amended) ~~Method~~The method according to ~~Patent C~~claim 1, ~~characterized by the~~ further ~~step of~~comprising:

d) carrying out an implantation ~~(I1)~~ in order to form connection doping regions ~~(LDD)~~ in the semiconductor substrate ~~(1)~~.

3. (Currently Amended) ~~Method~~The method according to ~~one of Patent Claims 1 and 2, characterized by the~~claim 1, further ~~step of~~comprising:

e) depositing a further insulation layer ~~(7)~~ selectively with respect to the deposition-inhibiting layers ~~(2A, 4)~~ in order to form a widened spacer structure.

4. (Currently Amended) ~~Method~~The method according to ~~Patent C~~claim 3, ~~characterized by the~~ further ~~step of~~comprising:

f) carrying out a further implantation ~~(I2)~~ in order to form source/drain regions ~~(S/D)~~ in the semiconductor substrate ~~(1)~~.

5. (Currently Amended) ~~Method~~The method according to ~~one of Patent Claims 1 to 4, characterized in that~~claim 1, wherein the deposition-inhibiting layers ~~(2A, 4)~~ include at least one of nitride layers and ~~/or~~ oxynitride layers with a high nitrogen content, and ozone-enhanced TEOS deposition is carried out in ~~step~~ c) ~~and/or step e)~~.

6. (Currently Amended) ~~Method~~The method according to ~~one of Patent Claims 1 to 5, characterized in that~~ claim 1, wherein the selectively deposited insulation layers ~~(6, 7)~~ at ~~the~~ side walls of the gate stack ~~(G)~~ have spacer layers ~~(S6, S7)~~ and at the deposition-inhibiting layers ~~(2A, 4)~~ have thin residual layers, the method comprising removing the residual layers ~~being removed~~ by wet etching ~~in a further step~~.

7. (Currently Amended) ~~Method~~The method according to ~~one of Patent Claims 1 to 6, characterized by the further step~~claim 1, further comprising ~~c1) and/or step e1) of~~ densifying the selectively deposited insulation layers ~~(6, 7)~~.

8. (Currently Amended) ~~Method~~The method according to ~~one of Patent Claims 1 to 7, characterized by the~~claim 1, further ~~steps of~~comprising:

g) removing the deposition-inhibiting layers ~~(2A, 4)~~ in order to uncover the gate layer ~~(3)~~ and the semiconductor substrate ~~(1)~~;

h) depositing a material which can be silicided; and

i) converting a surface layer of the uncovered semiconductor substrate ~~(1)~~ and the gate layer ~~(3)~~ using the material which can be silicided in order to form highly conductive connection regions ~~(8)~~ for ~~the~~ source/drain regions ~~(S/D)~~ and the gate layer ~~(3)~~.

9. (Currently Amended) ~~Method~~The method according to ~~one of Patent Claims 1 to 8, characterized in that~~claim 1, wherein the gate layer ~~(3)~~ includes polycrystalline silicon and the semiconductor substrate ~~(1)~~ includes crystalline silicon.

10. (Cancelled)

11. (New) The method according to claim 3, wherein the deposition-inhibiting layers include at least one of nitride layers and oxynitride layers with a high nitrogen content, and ozone-enhanced TEOS deposition is carried out in at least one of step c) and step e).

12. (New) The method according to claim 3, further comprising densifying one of the selectively deposited insulation layers in c) or e).

13. (New) A method of fabricating a sub-100 nanometer field-effect transistor, the method comprising fabricating a spacer structure, fabrication of the spacer structure comprising:

a) forming a gate insulation layer having a gate deposition-inhibiting layer, a gate layer and a covering deposition-inhibiting layer on a semiconductor substrate;

b) patterning the gate layer and the covering deposition-inhibiting layer in order to form gate stacks; and

c) depositing an insulation layer selectively with respect to the deposition-inhibiting layers to form the spacer structure.

14. (New) The method according to claim 13, further comprising:

d) carrying out an implantation in order to form connection doping regions in the semiconductor substrate.

15. (New) The method according to claim 13, further comprising:

e) depositing a further insulation layer selectively with respect to the deposition-inhibiting layers in order to form a widened spacer structure.

16. (New) The method according to claim 15, further comprising:

f) carrying out a further implantation in order to form source/drain regions in the semiconductor substrate.

17. (New) The method according to claim 13, wherein the deposition-inhibiting layers include at least one of nitride layers and oxynitride layers with a high nitrogen content, and ozone-enhanced TEOS deposition is carried out in c).

18. (New) The method according to claim 13, wherein the selectively deposited insulation layers at side walls of the gate stack have spacer layers and at the deposition-inhibiting layers have thin residual layers, the method comprising removing the residual layers by wet etching.

19. (New) The method according to claim 13, further comprising densifying the selectively deposited insulation layer.

20. (New) The method according to claim 13, further comprising:

g) removing the deposition-inhibiting layers in order to uncover the gate layer and the semiconductor substrate;

h) depositing a material which can be silicided; and

i) converting a surface layer of the uncovered semiconductor substrate and the gate layer using the material which can be silicided in order to form highly conductive connection regions for source/drain regions and the gate layer.

21. (New) The method according to claim 13, wherein the gate layer includes polycrystalline silicon and the semiconductor substrate includes crystalline silicon.

22. (New) The method according to claim 15, wherein the deposition-inhibiting layers include at least one of nitride layers and oxynitride layers with a high nitrogen content, and ozone-enhanced TEOS deposition is carried out in at least one of step c) and step e).

23. (New) The method according to claim 15, further comprising densifying one of the selectively deposited insulation layers in c) or e).